

```

Define [op_is_ =  $\varepsilon$ ] :=
Module [ {SD, ii, jj, kk, isp, nis, nisp, sis},
Block [ {i, j, k},
ReleaseHold [ Hold [
SD [ op_nisp, $k_Integer, Block [ {i, j, k}, op_isp, $k =  $\varepsilon$ ;
op_nis, $k ] ] ];
SD [ op_isp, op{is}, $k ] ; SD [ op_sis_, op{sis} ] ;
] /. {SD → SetDelayed,
isp → {is} /. {i → i_, j → j_, k → k_},
nis → {is} /. {i → ii, j → jj, k → kk},
nisp → {is} /. {i → ii_, j → jj_, k → kk_}
} ] ] ]

```