

```

SetAttributes[Define, HoldAll];
Define[def_, defs__] := (Define[def]; Define[defs]);
Define[op_is__ =  $\varepsilon$ _] := Module[{SD, ii, jj, kk, isp, nis, nisp, sis}, Block[{i, j, k},
  ReleaseHold[Hold[
    SD[op_nisp, $E_, PPBoot@Block[{i, j, k}, op_isp, $E =  $\varepsilon$ ; op_nis, $E]]];
    SD[op_isp, op_{is}, $E]; SD[op_sis__, op_{sis}];
  ] /. {SD → SetDelayed,
    isp → {is} /. {i → i_, j → j_, k → k_},
    nis → {is} /. {i → ii, j → jj, k → kk},
    nisp → {is} /. {i → ii_, j → jj_, k → kk_}
  } ] ]

```